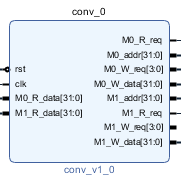
HOMEWORK 5

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**Design idea:**

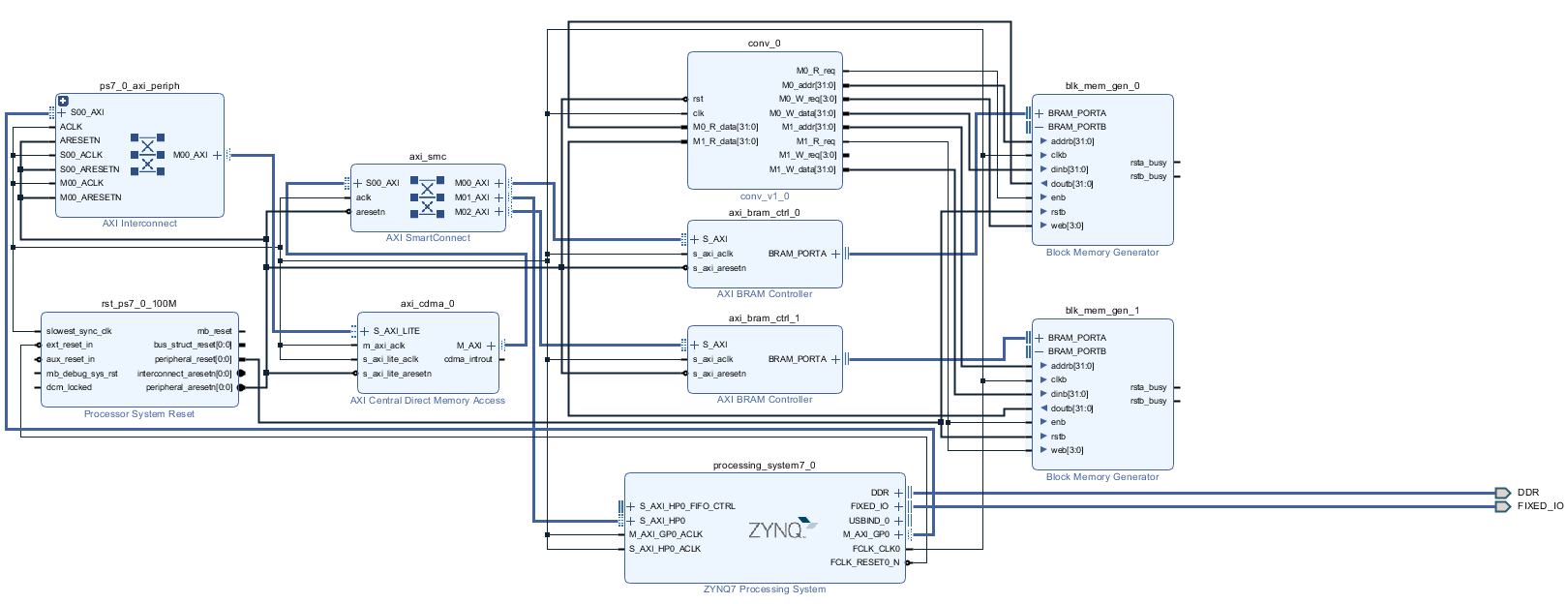
(Please describe the function and features of the convolution circuit)



First for all, I create a convolution has name is *conv\_v1\_0* that is connected to my system by IP. Its function that is read the input data and bias are taken from input.hex and execute convolution for that values. Besides that, I also used some knowledge from homework before to apply in this homework.

**Block design Screenshot:**

(Please attach a screenshot and describe the block design function.)

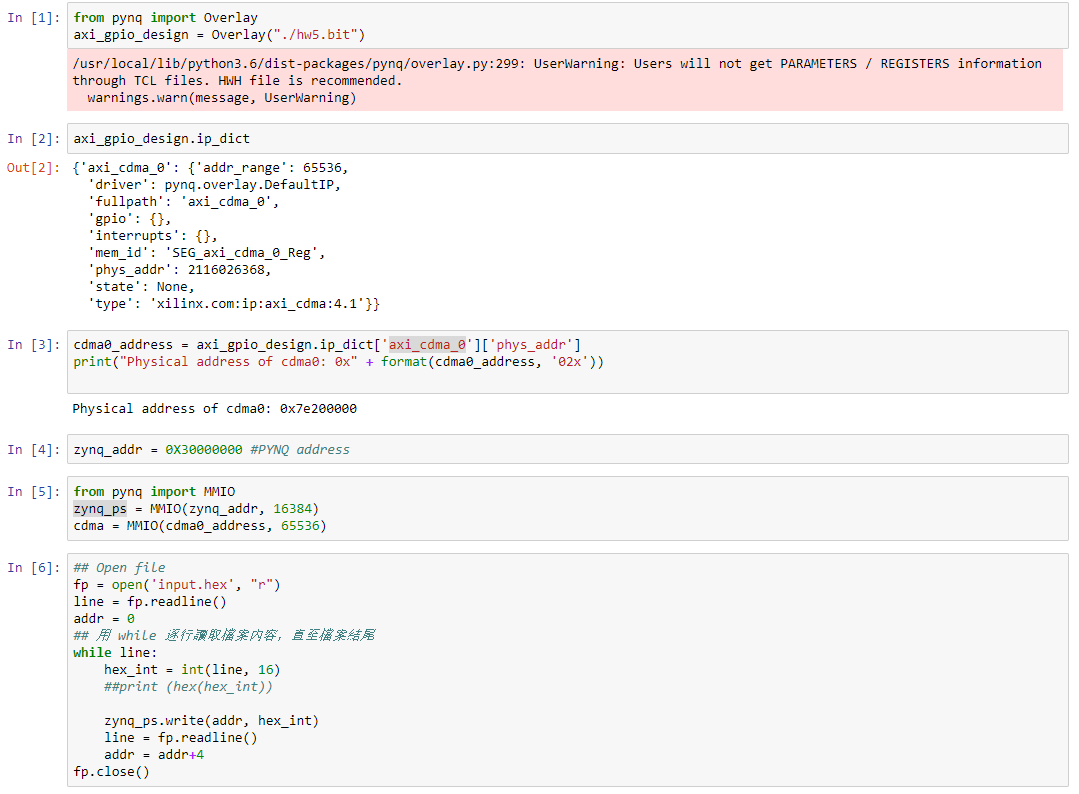


Besides the conv\_v1\_0 block, there are 6 main blocks in my system to execute requires that are: ZYNQ7 Processing system, AXI BRAM Controller, AXI Central Direct Memory Access, Processor system reset, Block Memory Generator and AXI Interconnect.

* ZYNQ7 Processing system: consists of a system-on-chip (SoC) style integrated processing system (PS) and a Programmable Logic (PL) unit, providing an extensible and flexible SoC solution on a single die.
* AXI BRAM Controller: The AXI Bram Controller is an IP provided by Xilinx Vivado. It mainly converts the block memory read and write signals into AXI format, allowing block memory to communicate with AXI BUS.
* AXI Central Direct Memory Access (CDMA): is an IP provided by Xilinx Vivado that can move data between two memory addresses. Like a normal DMA, CDMA has both Master and Slave pins on the system.
* Processor system reset: allows the customer to tailor the design to suit their application by setting certain parameters to enable/disable features.
* Block Memory Generator: is an IP provided by Xilinx Vivado, which can generate Block memory. It is similar to the general Sram. It can adjust various parameters, such as memory size, single port or dual port, etc. It is a bit like memory compiler, block memory.
* AXI Interconnect: connecting one or more AXI memory-mapped Master devices to one or more memory-mapped Slave devices.

**Jupyter python code:**

(Please describe the function and execution flow of the jupyter python code.)



* In the input [1], we read the hw5.bit which contains all information of hardware and it is exported by Vivado.
* In the input [2], we use a command that is “axi\_gpio\_design.ip\_dict” which is used to determine information in dictionary IPs. The important information is included that the IP driver, physical address, version.
* In the input [3], the cdma0\_address value is a dictionary mapping the physical address. The operation address of axi\_cdma\_0 is 0x7e200000.
* In the input [4] & [5], set the operating address of ZYNQ: zynq\_addr = 0X30000000. Use MMIO operation cmda and zynq\_ps.
* In the input [6] read the contents in *input.hex.*



* In the input [7] write data from ZYNQ to bram0
* In the input [8] write data from bram1 to ZYNQ
* In the input [9] write the output data to *output.hex*



* In the input [10] check values in the *output.hex* with *golden.hex*. If true, the word *CONGRATULATIONS!* will show.

**Lesson learn**

(Please write down the experience of completing this assignment, what you learned, and the points of difficulty.)

When I finished this homework, I learned many knowledges about design hardware by Vivado. Besides that, I can create a convolution system and process input data.

About Jupyter, I learned how to set address for cdma and zynq. From that. I can transfer value to block memory to calculate and receive the result to display.

The difficulty point, I must try to create a convolution block can connect with my processing system by IP. Further, using the test\_band file to test my code is compiled in convolution block.